

The circuit diagram illustrates a 1-bit digital-to-analog converter (DAC) implemented with a differential pair and two sample-and-hold stages. The input signal **DB** is connected to the gates of two NMOS transistors, **N1** and **N2**. The source of **N1** is connected to a PMOS transistor **P1**, which is tied to **Vcc**. The source of **N2** is connected to a PMOS transistor **P2**, which is also tied to **Vcc**. The drains of **N1** and **N2** are labeled **NODE A** and **NODE B**, respectively. **NODE A** is connected to a sample-and-hold stage **S.F.1** (71), and **NODE B** is connected to a sample-and-hold stage **S.F.2** (72). The outputs of **S.F.1** and **S.F.2** are connected to capacitors **C11** and **C12**, respectively. The other ends of **C11** and **C12** are connected to **NODE C**. **NODE C** is also connected to a PMOS transistor **P3**, whose gate is tied to **Vcc**. The drain of **P3** is connected to a resistor network consisting of **R1**, **R2**, and **R3** in series, with **R1** connected to **Vcc** and **R3** connected to ground. The node between **R2** and **R3** is labeled **Vref**. The output of the DAC is **Dout**, which is connected to the non-inverting input (+) of an operational amplifier (73). The inverting input (-) of the op-amp is connected to **Vref**. The op-amp is configured as a voltage follower, so its output is **Dout**. The op-amp is represented by a triangle with a '+' sign on the non-inverting input and a '-' sign on the inverting input. The output of the op-amp is labeled **Dout**.

FIG.3

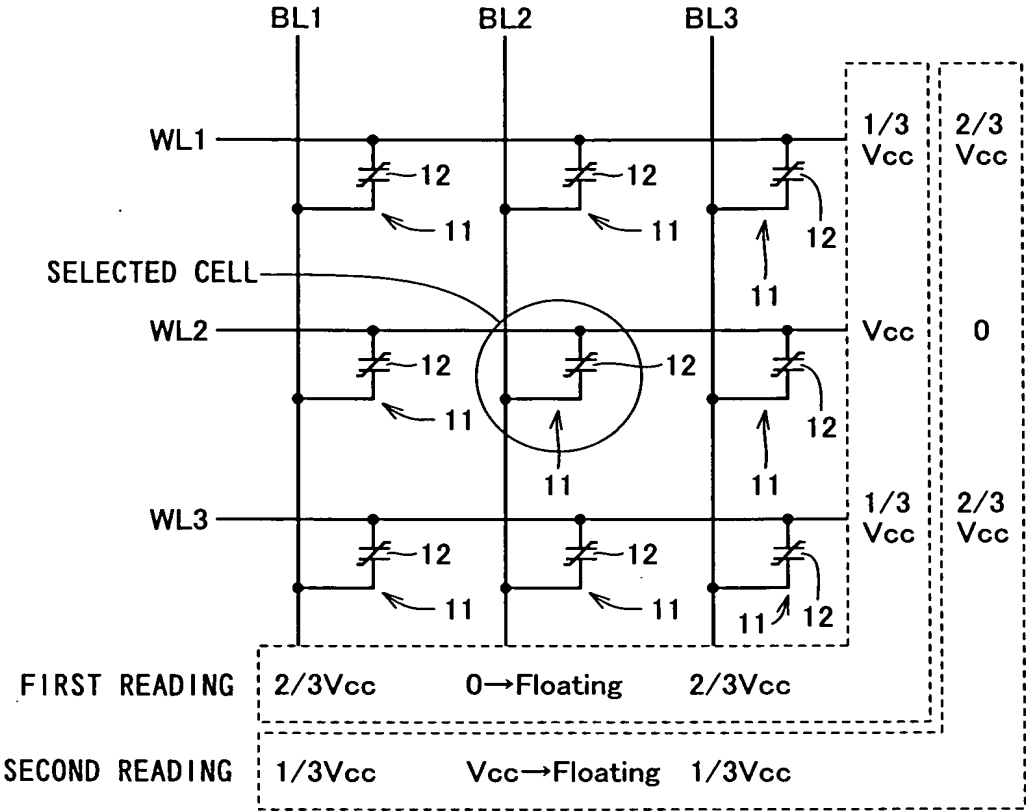


FIG.4

INITIAL DATA	FIRST VARIATION	DATA FOLLOWING FIRST READING	SECOND VARIATION	DATA FOLLOWING SECOND READING	VARIATION CORRESPONDING TO TWO READ OPERATIONS
0	ΔV_a	0	$-\Delta V_b$	1	$\Delta V_a - \Delta V_b < 0$
1	ΔV_b	0	$-\Delta V_b$	1	$\Delta V_b - \Delta V_b = 0$

FIG.5

FLOATING

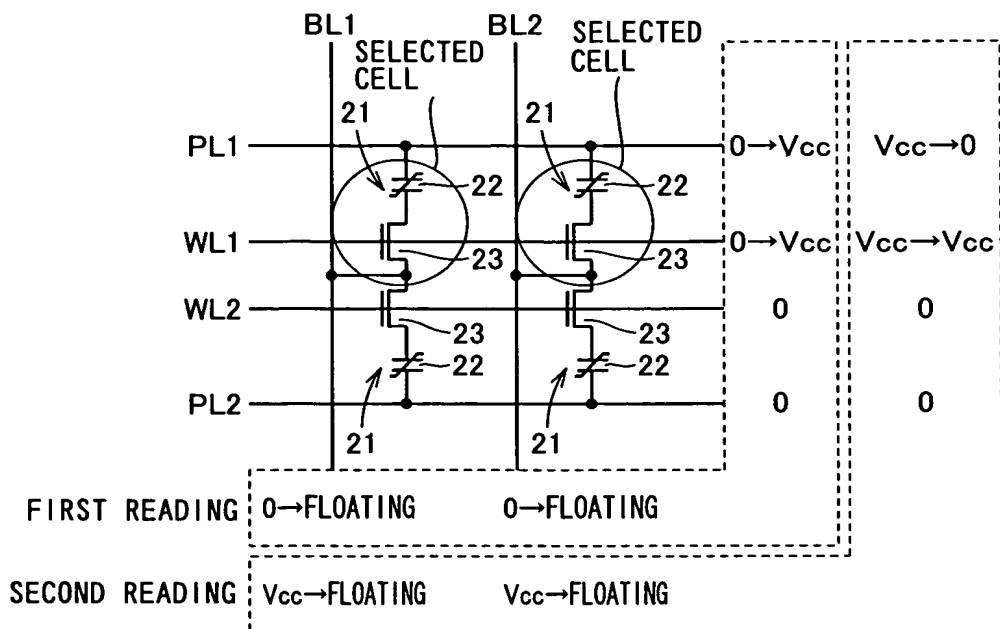


FIG.6

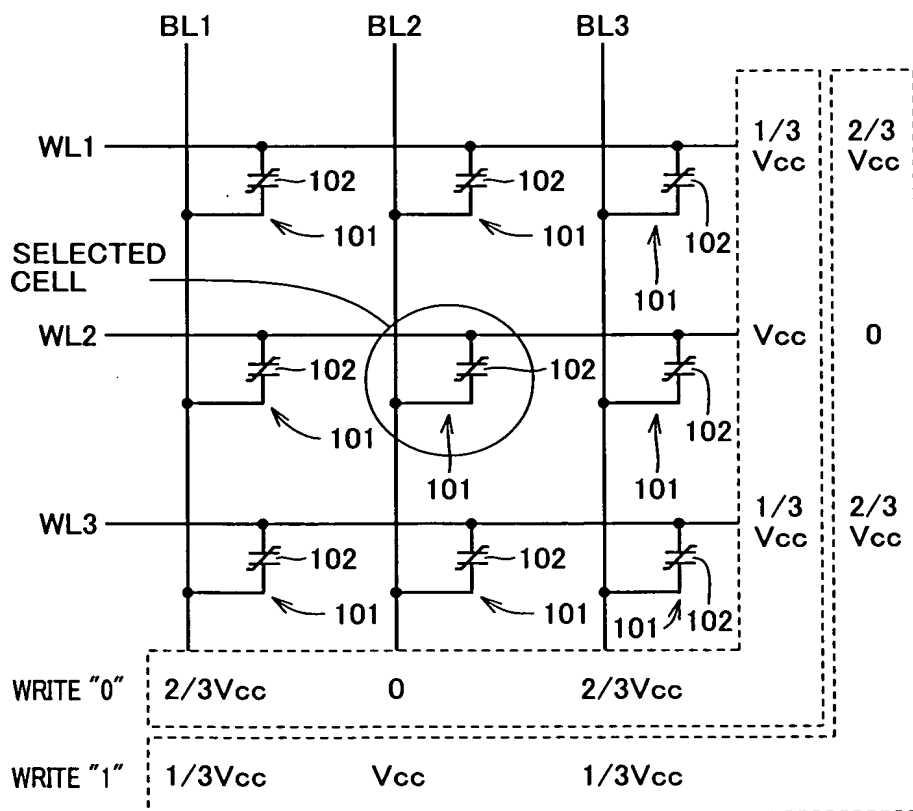


FIG. 7

